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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
KIM, HONG CHONG	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 03/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/829,146	TOOMBS ET AL.	
	Examiner	Art Unit	
	Hong C Kim	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-22 and 24-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-22 and 24-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 17-22, 24 –27, and 28-38 are presented for examination. This office action is in response to the RCE filed on 11/22/2004.

2. Again, applicants are requested to supply published previous versions (i.e. Version 1.0, 1.1, 1.2, and 1.3) of The MultiMediaCard System Specification and any publications related to The MultiMediaCard System because information are not readily available to the examiner.

3. The examiner requests, in response to this Office action, any reference(s) known to qualify as prior art under 35 U.S.C. sections 102 or 103 with respect to the invention as defined by the independent and dependent claims. That is, any prior art (including any products for sale) similar to the claimed invention that could reasonably be used in a 102 or 103 rejection. This request does not require applicant to perform a search. This **request** is not intended to interfere with or go beyond that **required** under 37 C.F.R. 1.56 or 1.105.

The request may be fulfilled by asking the attorney(s) of record handling prosecution and the inventor(s)/assignee for references qualifying as prior art. A simple statement that the query has been made and no prior art found is sufficient to fulfill the request. Otherwise, the fee and certification requirements of 37 CFR section 1.97 are waived for those documents submitted in reply to this request. This waiver extends only to those documents within the scope of this request that are included in the application's first complete communication responding to this requirement. Any supplemental replies

subsequent to the first communication responding to this request and any information disclosures beyond the scope of this are subject to the fee and certification requirements of 37 CFR section 1.97.

In the event prior art documentation is submitted, a discussion of relevant passages, figs. etc. with respect to the claims is requested. The examiner is looking for specific references to 102/103 prior art that identify independent and dependent claim limitations. Since applicant is most knowledgeable of the present invention and submitted art, his/her discussion of the reference(s) with respect to the instant claims is essential. **A response to this inquiry is greatly appreciated.**

The examiner also requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line number(s), in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The title should be more specific to differentiate the invention from similar inventions in the patent literature. "memory groups", " memory cells", "group tags", "erasable", and "write protected" aspects of the invention should be mentioned in the title so that the title is more descriptive.

Claim Objections

5. Claim 33 is objected to because of the following informalities: It appears that added limitation "in response too few tags being set, a received erase command is aborted" was not described in the specification at the time the application was filed, had possession of the claimed invention.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 24, 26, 34-36, 25, 27, and 37-38 are rejected under 35 U.S.C. 102(b) as being anticipated by Fandrich et al. (Fandrich) U.S. Patent 5,509,134 or Harari et al. (Harari) U.S. Patent 5,418,752.

As to claim 24, Fandrich discloses the invention as claimed. Fandrich discloses a memory system (Fig. 2) comprises a plurality of memory groups (col. 3 lines 55-60), each of said memory groups comprising a plurality of memory cells (col. 3 lines 55-60) in each memory group is configurable (Fig. 4 and col. 11 lines 28- 36) ; a plurality of group tags (col. 11 lines 29-38, lock bits, and Fig. 3 Ref. 260), each of said group tags corresponding to one of said memory groups, each of said group tags indicating whether the memory cells under the corresponding memory group are write protected

(col. 11 lines 29-38 and Fig. 3 Ref. 260); and wherein any combination of the memory groups can be write protected (col. 11 lines 29-38, "corresponding blocks" read on this limitation and Fig. 3 Ref. 260).

Alternatively, Harari discloses the invention as claimed. Harari discloses a memory system (Fig. 1B) comprises a plurality of memory groups (Fig. 1 Refs, 43-47, col. 1 line 61 thru col. 2 line 1), each of said memory groups comprising a plurality of memory cells (Fig. 1 Refs. 211, 213, 215, & 217) in each memory group is configurable (col. 5 lines 25+, col. 7 lines 13-19, and Fig. 1); a plurality of group tags (col. 6 lines 41-46), each of said group tags corresponding to one of said memory groups, each of said group tags indicating whether the memory cells under the corresponding memory group are write protected (col. 6 lines 41-46); and wherein any combination of the memory groups can be write protected (col. 1 line 61 thru col. 2 line 1 and col. 5 lines 1-5).

As to claim 25, Fandrich discloses the invention as claimed. Fandrich discloses a memory system (Fig. 2) comprises a plurality of memory groups (col. 3 lines 55-60), each of said memory groups comprising a plurality of memory cells (col. 3 lines 55-60) in each memory group are calculated in real time (Fig. 4 and col. 11 lines 28- 36, setting and reading status bit reads on this limitation) ; a plurality of group tags (col. 11 lines 29-38, lock bits, and Fig. 3 Ref. 260), each of said group tags corresponding to one of said memory groups, each of said group tags indicating whether the memory cells under the corresponding memory group are write protected (col. 11 lines 29-38 and Fig. 3 Ref.

260); and wherein any combination of the memory groups can be write protected (col. 11 lines 29-38, "corresponding blocks" read on this limitation and Fig. 3 Ref. 260).

Alternatively, Harari discloses the invention as claimed. Harari discloses a memory system (Fig. 1B) comprises a plurality of memory groups (Fig. 1 Refs, 43-47, col. 1 line 61 thru col. 2 line 1), each of said memory groups comprising a plurality of memory cells (Fig. 1 Refs. 211, 213, 215, & 217) in each memory group are calculated in real time (col. 5 lines 25+, setting command register, decoding reads on this limitation and col. 7 lines 13-19); a plurality of group tags (col. 6 lines 41-46), each of said group tags corresponding to one of said memory groups, each of said group tags indicating whether the memory cells under the corresponding memory group are write protected (col. 6 lines 41-46); and wherein any combination of the memory groups can be write protected (col. 1 line 61 thru col. 2 line 1 and col. 5 lines 1-5).

As to claims 26 and 27, Fandrich further discloses a flash memory (Fig. 2 Ref. 20). Harari further discloses a flash memory (Fig. 1 Ref. 33).

As to claim 34, Fandrich further discloses wherein said group tags are settable by a host to which the memory system is connected (Fig. 4b). Harari further discloses wherein said group tags are settable by a host to which the memory system is connected (col. 5 lines 25+ and col. 7 lines 13-19).

As to claim 35, Fandrich further discloses wherein said group tags are set in response to a host command (Fig. 4b). Harari further discloses wherein said group tags are set (col. 5 lines 25+, setting command register, decoding reads on this limitation and col. 7 lines 13-19) in response to a host command (Fig. 3A Ref. 225).

As to claim 36, Fandrich further discloses wherein set ones of said group tags are deselected in response to a host command (Fig. 4b). Harari further discloses wherein set ones of said group tags are deselected (col. 5 lines 25+, selecting(deselecting) and decoding reads on this limitation and col. 7 lines 13-19) in response to a host command (Fig. 3A Ref. 225).

As to claim 37,Fandrich discloses the invention as claimed. Fandrich discloses a memory system (Fig. 2) comprises a plurality of memory groups (col. 3 lines 55-60), each of said memory groups comprising a plurality of memory cells (col. 3 lines 55-60); a plurality of group tags (col. 11 lines 29-38, lock bits, and Fig. 3 Ref. 260), each of said group tags corresponding to one of said memory groups, each of said group tags indicating whether the memory cells under the corresponding memory group are write protected (col. 11 lines 29-38 and Fig. 3 Ref. 260); and wherein any combination of the memory groups can be write protected (col. 11 lines 29-38, "corresponding blocks" read on this limitation and Fig. 3 Ref. 260) and said group tags are settable in response to a command (Fig. 4b) from a host to which the memory system is connected.

Alternatively, Harari discloses the invention as claimed. Harari discloses a memory system (Fig. 1B) comprises a plurality of memory groups (Fig. 1 Refs, 43-47, col. 1 line 61 thru col. 2 line 1), each of said memory groups comprising a plurality of memory cells (Fig. 1 Refs. 211, 213, 215, & 217); a plurality of group tags (col. 6 lines 41-46), each of said group tags corresponding to one of said memory groups, each of said group tags indicating whether the memory cells under the corresponding memory group are write protected (col. 6 lines 41-46); and wherein any combination of the memory groups can be write protected (col. 1 line 61 thru col. 2 line 1 and col. 5 lines 1-5) and said group tags are settable in response to a command (Fig. 3A Ref. 225) from a host to which the memory system is connected.

As to claim 38, Fandrich further discloses set ones said group tags are deselected in response to command from said host (Fig. 4b). Harari further discloses set ones said group tags are deselected in response to command from said host (Fig. 3A Ref. 225).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Alternatively, claims 24-27 and 34-36 are rejected under 35 U.S.C. 103(a) as

being unpatentable over Fandrich et al. (Fandrich) U.S. Patent 5,509,134 or Harari et al. (Harari) U.S. Patent 5,418,752 in view of Kishi et al. (Kishi) U.S. Patent No. 4,841,432 or Noel et al. (Noel) U.S. Pub. No. 2002/00168891.

As to claim 24, Fandrich discloses a memory system (Fig. 2) comprises a plurality of memory groups (col. 3 lines 55-60), each of the memory groups comprising a plurality of memory cells (col. 3 lines 55-60); a plurality of group tags (col. 11 lines 29-38, lock bits, and Fig. 3 Ref. 260), each of the group tags corresponding to one of the memory groups, each of the group tags indicating whether the memory cells under the corresponding memory group are write protected (col. 11 lines 29-38 and Fig. 3 Ref. 260); and wherein any combination of the memory groups can be write protected (col. 11 lines 29-38, "corresponding blocks" read on this limitation and Fig. 3 Ref. 260). Even if Fandrich does not specifically disclose the number of memory cells in each memory group is configurable. Kishi discloses the number of memory cells in each memory group is configurable (abstract) for the purpose of optimizing configuration of the memory.

Therefore, it would have been obvious to one having ordinary skill in the memory art at the time the invention was made to incorporate the number of memory cells in each memory group is configurable as shown in Kishi into the invention of Fandrich because it would optimize configuration of the memory.

Alternatively, Noel discloses the number of memory cells in each memory group is configurable (block 265) for the purpose of optimizing configuration of the memory.

Therefore, it would have been obvious to one having ordinary skill in the memory art at the time the invention was made to incorporate the number of memory cells in each memory group is configurable as shown in Noel into the invention of Fandrich because it would optimize configuration of the memory.

As to claim 34, Fandrich further discloses wherein said group tags are settable by a host to which the memory system is connected (Fig. 4b).

As to claim 35, Fandrich further discloses wherein said group tags are set in response to a host command (Fig. 4b).

As to claim 36, Fandrich further discloses wherein set ones of said group tags are deselected in response to a host command (Fig. 4b).

As to claim 25, Kishi further discloses the corresponding cells in each memory groups is calculated in real time (col. 5 lines 32-42, program reads on this limitation, since it runs during the real time). Alternatively, Noel further discloses the corresponding cell in each memory groups is calculated in real time (block 265, software configuration reads on this limitation, since it runs during the real time).

As to claims 26 and 27, Fandrich further discloses a flash memory (Fig. 2 Ref. 20).

8. Claims 17–19, 31, 20, 21, 32, 22, 28-30, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harari et al. (Harari) U.S. Patent 5,418,752 in view of Kaki et al. (Kaki) U. S. Patent 5,809,515.

As to claim 17, Harari discloses a memory system (Fig. 1B) comprises a plurality of memory groups, each of the memory groups comprising a plurality of memory sectors, each of the memory sectors (col. 1 line 61 thru col. 2 line 1) comprising a plurality of memory cells; a plurality of sector tags, each of the sector tags corresponds to a memory sector, each of the sector tags (col. 6 lines 41-46) indicating whether the memory cells under the corresponding memory sector are erasable, wherein al the memory cells belong to one memory sector are erasable when the corresponding sector tag is set, wherein any combination of memory sectors in a memory group can be simultaneously erased (col. 5 lines 1-5 and col. 1 line 61 thru col. 2 line 1). Although Harari discloses the entire chip is erased at one time (col. 4 lines 47+) and permits selection of sectors across various chips for simultaneous ease (col. 6 lines 1-2), however, Harari does not specifically disclose a plurality of group tags, each of the group tags corresponds to one of the memory groups, each of the group tags indicating whether the memory cells under the corresponding memory group are erasable, wherein al the memory cells belong to one memory group are erasable when the corresponding group is set, wherein any combination of memory groups can be simultaneously erased.

Kaki discloses a plurality of group tags, each of the group tags corresponds to one of the memory groups, each of the group tags indicating whether the memory cells under the corresponding memory group are erasable (col. 7 line 64 thru col. 8 line 14), wherein all the memory cells belong to one memory group are erasable when the corresponding group is set, wherein any combination of memory groups can be simultaneously erased (col. 7 lines 28-30, "Thus, the plurality of flash memories 4 are erased in parallel" reads on this limitation) for the purpose of increasing the memory erasing speed thereby increasing the access bandwidth.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate plurality of group tags, each of the group tags corresponds to one of the memory groups, each of the group tags indicating whether the memory cells under the corresponding memory group are erasable, wherein all the memory cells belong to one memory group are erasable when the corresponding group is set, wherein any combination of memory groups can be simultaneously erased as shown in Kaki into the invention of Harari because it would increase the memory access speed.

As to claim 18, Harari and Kaki disclose the invention as claimed above. Harari discloses the number of memory sectors in each memory group is configurable (col. 5 lines 25+ and col. 7 lines 13-19).

As to claim 19, Harari further discloses the corresponding sectors in each memory group is calculated in real time (col. 5 lines 25+, setting command register, decoding reads on this limitation and col. 7 lines 13-19).

As to claim 31, Harari further discloses wherein the number of memory sectors in each memory group is configurable (col. 5 lines 25+, col. 7 lines 13-19, and Fig. 1) by a host to which the memory system is connected.

As to claim 20, Harari and Kaki disclose the invention as claimed above. Harari discloses the number of memory cells in each memory sector is configurable (col. 5 lines 25+ and col. 7 lines 13-19).

As to claim 21, Harari further discloses the corresponding cells in each memory sector is calculated in real time (col. 5 lines 25+, setting command register, decoding reads on this limitation and col. 7 lines 13-19).

As to claim 32, Harari further discloses wherein the number of memory cells in each memory sector is configurable (col. 5 lines 25+, col. 7 lines 13-19, and Fig. 1) by a host to which the memory system is connected.

As to claim 22, Harari further discloses a flash memory (abstract line 1)

As to claim 28, Harari and Kaki disclose the invention as claimed above. The sector tags (disclosed by Harari col. 6 lines 41-45 and col.5 lines 25+, Fig. 1) and the group tags (disclosed by Kaki Fig. 4 Refs. 42-47) are settable by a host to which the memory system is connected.

As to claim 29, Harari and Kaki disclose the invention as claimed above. The sector tags (disclosed by Harari col. 6 lines 41-45 and col. 5 lines 25+, Fig. 1) and the group tags (disclosed by Kaki Fig. 4 Refs. 42-47) are set in response to a host command.

As to claim 30, Harari and Kaki disclose the invention as claimed above. The sector tags (disclosed by Harari col. 6 lines 41-45 and col. 5 lines 25+, Fig. 1) and the group tags (disclosed by Kaki Fig. 4 Refs. 42-47) are deselected in response to a host command.

As to claim 33, Harari further discloses wherein in response to too few tags being set a received erase command is aborted (col. 5 – col. 6 not setting any sector reads on this limitation, col. 6 lines 61+, and col. 7 lines 1-11) .

9. Alternatively, claims 18-22 and 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harari et al. (Harari) U.S. Patent 5,418,752 in view of Kaki et al. (Kaki) U. S. Patent 5,809,515 and further in view of Kishi et al. (Kishi) U.S. Patent

No. 4,841,432 or Noel et al. (Noel) U.S. Pub. No. 2002/0016891.

As to claim 18, Harari and Kaki disclose the invention as claimed above. Even if neither Harari nor Kaki specifically discloses the number of memory sectors in each memory group is configurable. Kishi discloses the number of memory sectors in each memory group is configurable (abstract) for the purpose of optimizing memory configuration.

Therefore, it would have been obvious to one having ordinary skill in the memory art at the time the invention was made to incorporate the number of memory cells in each memory group is configurable as shown in Kishi into the combined invention of Harari and Kaki because it would optimize configuration of the memory devices.

Alternatively, Noel discloses the number of memory sectors in each memory group is configurable (block 265) for the purpose of optimizing memory configuration.

Therefore, it would have been obvious to one having ordinary skill in the memory art at the time the invention was made to incorporate the number of memory sectors in each memory group is configurable as shown in Noel into the combined invention of Harari and Kaki because it would optimize configuration of the memory devices.

As to claim 19, Kishi further discloses the corresponding sectors in each memory group is calculated in real time (col. 5 lines 32-42, program reads on this limitation, since it runs during the real time). Alternatively, Noel further discloses the corresponding sectors in each memory groups is calculated in real time (block 265, software configuration reads on this limitation, since it runs during the real time).

As to claim 31, Kishi further discloses wherein the number of memory sectors in each memory group is configurable (abstract) by a host to which the memory system is connected. Noel discloses wherein the number of memory sectors in each memory group is configurable (block 265) by a host to which the memory system is connected.

As to claim 20, Harari and Kaki disclose the invention as claimed above. Even if neither Harari nor Kaki specifically discloses the number of memory cells in each memory sector is configurable. Kishi discloses the number of memory cells in each memory sector is configurable (abstract) for the purpose of optimizing memory configuration.

Therefore, it would have been obvious to one having ordinary skill in the memory art at the time the invention was made to incorporate the number of memory cells in each memory sector is configurable as shown in Kishi into the combined invention of Harari and Kaki because it would optimize configuration of the memory devices.

Alternatively, Noel discloses the number of memory cells in each memory sector is configurable (block 265) for the purpose of optimizing memory configuration.

Therefore, it would have been obvious to one having ordinary skill in the memory art at the time the invention was made to incorporate the number of memory cells in each memory sector is configurable as shown in Noel into the combined invention of Harari and Kaki because it would optimize memory configuration.

As to claim 21, Kishi further discloses the corresponding cells in each memory sector is calculated in real time (col. 5 lines 32-42, program reads on this limitation, since it runs during the real time). Alternatively, Noel further discloses the corresponding cells in each memory sector is calculated in real time (block 265, software configuration reads on this limitation, since it runs during the real time).

As to claim 32, Kishi further discloses wherein the number of memory cells in each memory sector is configurable (abstract) by a host to which the memory system is connected. Noel further discloses wherein the number of memory cells in each memory sector is configurable (block 265) by a host to which the memory system is connected.

As to claim 22, Harari further discloses a flash memory (abstract line 1)

Response to Amendment

10. Applicant's arguments filed on 11/22/2004 have been fully considered but they are not deemed to be persuasive.

Applicant's remarks that the references not teaching wherein any combination of memory sectors in a memory group can be simultaneously erased.

Harari discloses wherein any combination of memory sectors in a memory group can be simultaneously erased (col. 5 lines 1-5, col. 6 lines 1-2 and col. 1 line 61 thru col. 2 line 1).

Applicant's remarks that the references not teaching wherein any combination of memory groups can be simultaneously erased.

Harari discloses the entire chip is erased at one time (col. 4 lines 47+) and permits selection of sectors across various chips for simultaneous ease (col. 6 lines 1-2, col. 5 lines 1-5 and col. 1 line 61 thru col. 2 line 1) and Kaki further discloses wherein any combination of memory groups can be simultaneously erased (col. 7 lines 28-30, "Thus, the plurality of flash memories 4 are erased in parallel" reads on this limitation).

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Therefore broadly written claims are disclosed by the references cited.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

2. A shortened statutory period for response to this action is set to expire 3 (three)

months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

3. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

4. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong Kim whose telephone number is (571) 272-4181. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 whose telephone number is (571) 272-2100.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7. **Any response to this action should be mailed to:**

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to TC-2100:
(703) 872-9306

Hand-delivered responses should be brought to the Customer Service Window (Randolph Building, 401 Dulany Street, Alexandria, VA 22314).

H Kim
Primary Patent Examiner
March 3, 2005